Avalon® to External Bus Bridge

For Quartus® Prime 18.1

1 Core Overview

The Avalon to External Bus Bridge provides a simple interface for a peripheral device to connect to the Avalon® Switch Fabric as a slave device. The bridge creates a bus-like interface to which one or more "slave" peripherals can be connected.

2 Functional Description

Figure 1 shows a block diagram of the Avalon to External Bus Bridge and its connections to the Avalon Switch Fabric and an external peripheral.

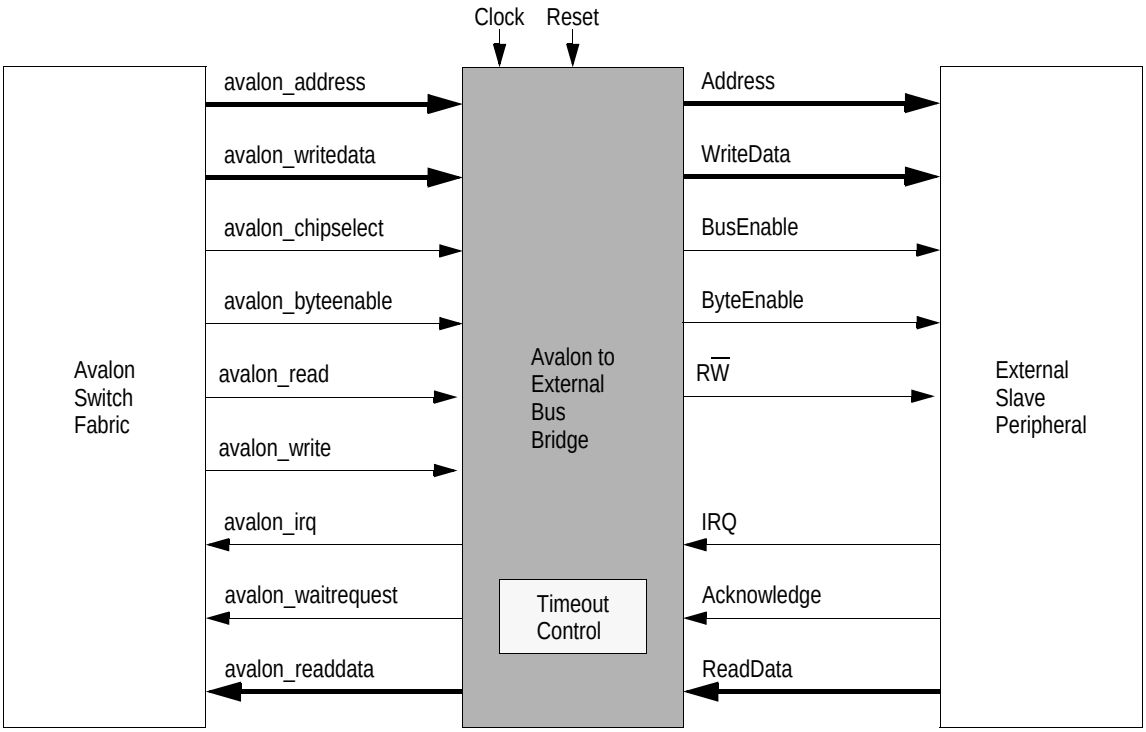

Figure 1. Avalon to External Bus Bridge Block Diagram

The bus signals provided are:

- Address — k bits (up to 32). The address of the data to be transferred. The address is aligned to the data size. For 32-bit data, the address bits $Address_{1-0}$ are equal to 0. The ByteEnable signals can be used to transfer less than 4 bytes.
- WriteData — 128, 64, 32, 16 or 8 bits. The data to be written to the peripheral device during a Write transfer.
- BusEnable — 1 bit. Indicates that all other signals are valid, and a data transfer should occur.
- ByteEnable — 16, 8, 4, 2 or 1 bits. Each bit indicates whether or not the corresponding byte should be read or written. These signals are active high.
- R$\overline{W}$ — 1 bit. Indicates whether the data transfer is a Read (1) or a Write (0) operation.
- IRQ — 1 bit. Used by the peripheral device to interrupt the Nios II processor.
- Acknowledge — 1 bit. Used by the peripheral device to indicate that it has completed the data transfer.
- ReadData — 128, 64, 32, 16 or 8 bits. The data that is read from the peripheral device during a Read transfer.

The bus is synchronous – all bus signals to the peripheral device must be read on the rising edge of the clock. To initiate a transfer, the *Address*, $R\overline{W}$, *ByteEnable* and possibly *WriteData* signals are set to the appropriate values. Then, the *BusEnable* signal is set to 1.

If the $R\overline{W}$ signal is 1, then the transfer is a Read operation and the peripheral device must set the *ReadData* signals to the appropriate values and set the *Acknowledge* signal to 1. The *Acknowledge* signal must remain at 1 for only one clock cycle. The *ReadData* signals must be constant while the *Acknowledge* signal is being asserted. Note that the reason why the *Acknowledge* signal must be high for exactly one clock cycle is that if this signal spans two or more cycles it may be interpreted by the Avalon Switch Fabric as corresponding to another transaction.

If the $R\overline{W}$ signal is 0, then the transfer is a Write operation and the peripheral device should write the value on the *WriteData* lines to the appropriate location. Once the peripheral device has completed the Write transfer, it must assert the *Acknowledge* signal for one clock cycle.

Figure 2 shows an example of the bridge that connects a Nios® II system implemented on the Intel® DE2 Board to a slave peripheral.

The Avalon to External Bus Bridge contains a time-out mechanism. If the peripheral takes too long to respond, the bridge will time out the communication so that the Avalon Switch Fabric will not get stalled. The timing of the Avalon to External Bus Bridge is similar to the System interconnect fabric, and the user can refer to the System Interconnect Fabric for Memory-Mapped Interfaces chapter in the Quartus® Prime Handbook or the Avalon Memory-Mapped Interface Specification for more information. As signals are registered inside the Avalon to External Bus Bridge, one clock cycle delay for write operations and a two clock cycle delay for read operations will be introduced.

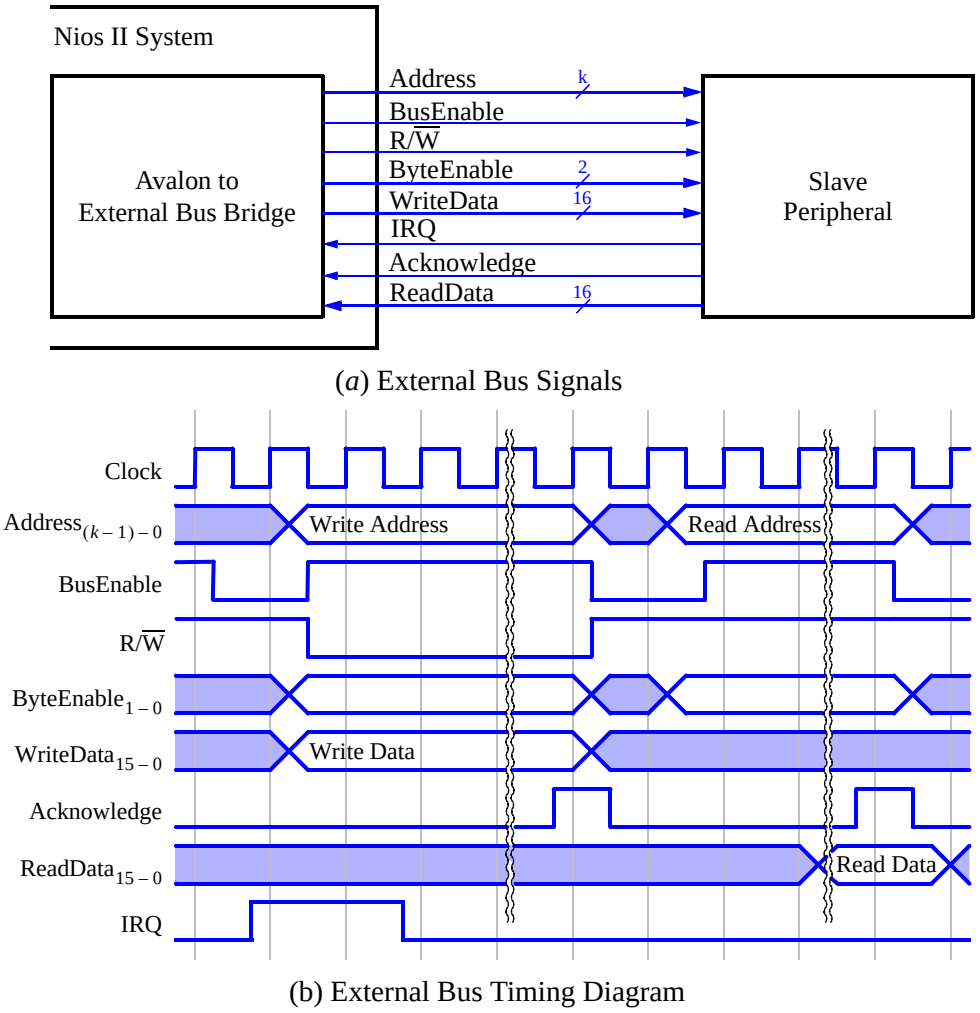

Figure 2. The Avalon to External Bus Bridge signals

3 Instantiating the Core in Platform Designer

Designers use the Avalon to External Bus Bridge's Configuration wizard in Platform Designer to specify the following parameters:

Data Width — The number of data bits involved in a transfer. The Bridge supports data widths of 8, 16, 32, 64 and 128 bits.

Address Range — The addressable space supported by the Bridge. It is possible to specify the address range of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512 and 1024, in either bytes, kilobytes (KBs) or megabytes (MBs).

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